Volume Production Testing of Silicon Photonics Modules Case Study: Wafer Sort Test Coverage versus Through-Put

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Abstract

Lowering Cost-Of-Test during volume production of Silicon Photonic products is directly proportional to lowering the Cost-Of-Manufacturing. A high-volume production test strategy which employs little or no wafer level test coverage prior to packaging results in low yield final assembly products. The cost of packaging defective die significantly increases the overall Cost-of-Manufacturing for the yielding final assembly products.

Employing a stringent full coverage wafer level test strategy during the production test process results in lengthy test times & very low through-put. This test strategy minimizes the possibility of packaging defective die, but due to the low through-put contributes to a significantly higher Cost-of-Test.

This case study describes a silicon photonic high-volume wafer sort test strategy which was implemented with the key objectives of: (1) providing enough wafer level test coverage to minimize packaging defective die; (2) maximize the wafer level test through-put; and (3) minimize the overall Cost-of-Test and Cost-of-Manufacturing.